Audio Platform

USB 2.0 Audio Design Platform

v. 1.10

OVERVIEW

The USB 2.0 Audio Design Platform is a complete, integrated solution, dedicated to be used in USB based Audio Devices, such as speakers or microphones.

The complete Audio Design Platform includes:

- DUSB2 peripheral controller designed to support 12 Mb/s “Full Speed” (FS) and 480 Mb/s “High Speed” (HS) serial data transmission rates
- DP8051XP ultra high performance, speed optimized, fully customizable 8051 8-bit microcontroller with built-in **DoCD™** debug IP core
- Audio Device stack-optimized software for DP8051XP 8-bit CPU
- FPGA board with ready to use, pre-programmed example USB stereo speakers application
- HAD2 – **DoCD™** Hardware Assisted Debugger board
- **DoCD™** Debug Software
- **DoCD™** driver for Keil development software
- **DoCD™** driver for IAR development software

MAIN FEATURES

- Full compliance with the USB 2.0 specification
- Full-speed 12 Mbps operation
- High-speed 480 Mbps operation
- Supports UTMI Transceiver Macrocell Interface
- Suspend and resume power management functions
- 100% software compatible with 8051 industry standard
- Up to 256 bytes of internal (on-chip) Data Memory
- Up to 64K bytes of internal (on-chip) or external (off-chip) Program Memory
- Up to 16M bytes of external (off-chip) Data Memory
- User programmable Program Memory Wait States solution for wide range of memories speed
- User programmable External Data Memory Wait States solution for wide range of memories speed
- Fully synthesizable, static synchronous design with positive edge clocking and no internal tri-states
- Scan test ready

DELIVERABLES

- DUSB2 & DP8051XP source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF netlist
- DUSB2 & DP8051XP test bench environments
  - NCSim automatic simulation macros
  - ModelSim automatic simulation macros
  - Active-HDL automatic simulation macros
  - Tests with reference responses
- Audio Devices software stack source code
- FPGA board with ready to use, preprogrammed example application

- HAD2 - **DoCD™** Hardware Assisted Debugger board
- **DoCD™** Debug Software
- **DoCD™** driver for Keil development software
- **DoCD™** driver for IAR development software
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods, without royalty-per-chip fees, make using of IP Core easy and simple.

Single Site license option – it is dedicated for small and middle sized companies, running their business at one location.

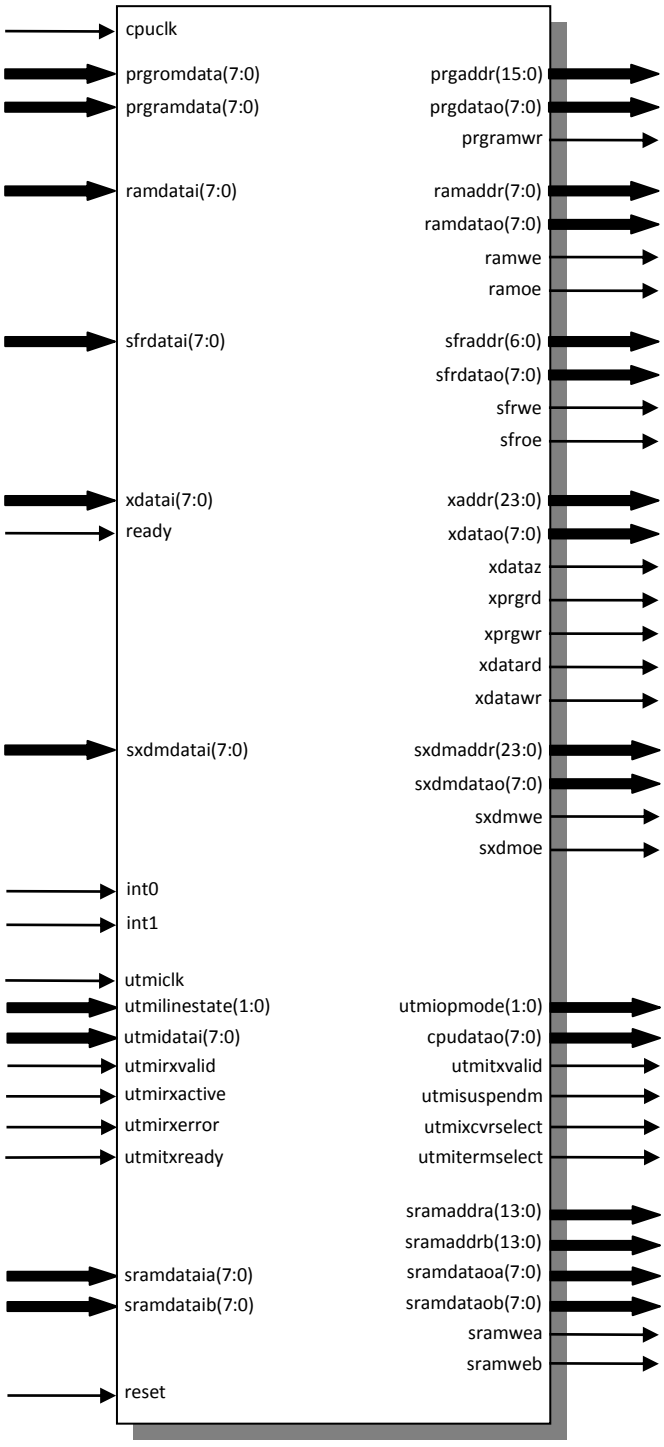
Multi Sites license option – it is dedicated for corporate customers, running their business at several places. Licensed product can be used in selected company branches.

In all cases, number of IP Core instantiation within a project and number of manufactured chips are unlimited. The license is royalty-per-chip free. There is no restrictions regarding the time of use.

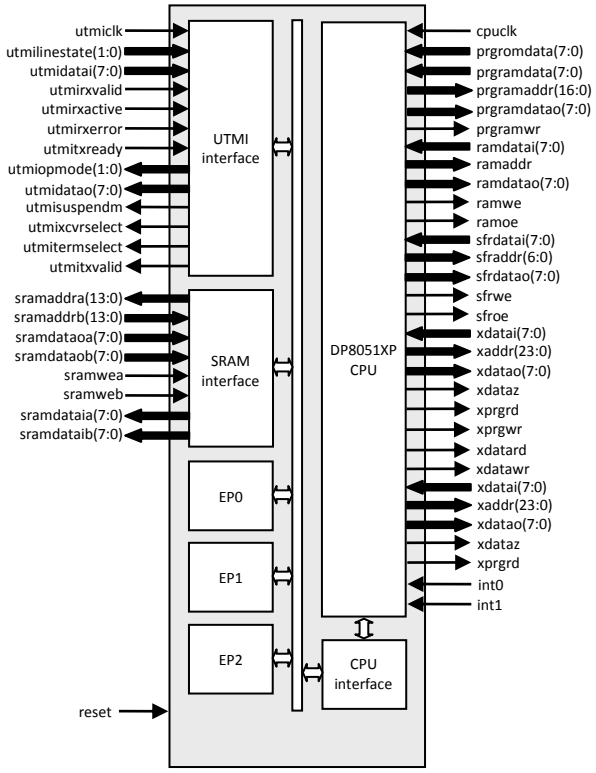
There are two formats of delivered IP Core:

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

SYMBOL



BLOCK DIAGRAM



PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
reset	input	Global reset
utmiclk	input	USB clock
utmilinestate(1:0)	input	USB line state
utmidatai(7:0)	input	USB parallel data input bus
utmirxvalid	input	USB receive valid
utmirxactive	input	USB receive active
utmirxerror	input	USB receive error
utmitxready	input	USB transmit ready
sramdataia(7:0)	input	SRAM port A data input bus
sramdataib(7:0)	input	SRAM port B data input bus
cpuclk	input	CPU clock
prgramdata[7:0]	input	Data bus from internal RAM program memory
prgromdata[7:0]	input	Data bus from internal ROM progogram memory
ramdatai[7:0]	input	Data bus from internal data memory

PIN	TYPE	DESCRIPTION
sfrdatai[7:0]	input	Data bus from user SFR's
xdatai[7:0]	input	Data bus from external memories
int0	input	External interrupt 0
int1	input	External interrupt 1
utmiopmode(1:0)	output	USB operational mode
utmidatao(7:0)	output	USB parallel data output bus
utmisuspendm	output	USB suspend
utmixcvrselect	output	USB transceiver select
utmitermselect	output	USB termination select
utmitxvalid	output	USB transmit valid
sramaddra(13:0)	output	SRAM port A address bus
sramaddrb(13:0)	output	SRAM port B address bus
sramdataoa(7:0)	output	SRAM port A data output bus
sramdataob(7:0)	output	SRAM port B data output bus
sramwea	output	SRAM port A write enable
sramweb	output	SRAM port B write enable
prgaddr[15:0]	output	Internal program memory address bus
prgdatao[7:0]	output	Data bus for internal program memory
prgramwr	output	Internal program memory write
ramaddr[7:0]	output	Internal Data Memory address bus
ramdatao[7:0]	output	Data bus for internal data memory
ramoe	output	Internal data memory output enable
ramwe	output	Internal data memory write enable
sfraddr[6:0]	output	Address bus for user SFR's
sfrdatao[7:0]	output	Data bus for user SFR's
sfroe	output	User SFR's output enable
sfrwe	output	User SFR's write enable
xaddr[23:0]	output	Address bus for external memories
xdatao[7:0]	output	Data bus for external memories
xdataz	output	Turn xdata bus into 'Z' state
xprgrd	output	External program memory read
xprgwr	output	External program memory write
xdatard	output	External data memory read
xdatawr	output	External data memory write

UNITS SUMMARY

UTMI Interface – This module is clocked by utmiclk clock and manages communication with USB 2.0 Transceiver Macrocell. It is responsible for reset detection, speed handshake, token, data and handshake packet reception and transmission.

CPU Interface – This module is clocked by cpuclk clock and manages communication with DP8051XP CPU. In this module DUSB2 core configuration and status registers are located.

SRAM Interface – This module manages communication with Synchronous Random Access Memory. It generates address, read and write signals for the SRAM memory and buffers data bytes during the FIFO read and write operations.

EP0 endpoint –The EP0 control endpoint is special bidirectional endpoint used for device configuration and allows generic USB control and status access.

EP1 endpoint – The EP1 data endpoint is unidirectional configurable endpoint used for application specific data transmission.

DP8051XP CPU – Ultra high performance, speed optimized 8-bit embedded controller, 100% software compatible with industry standard 8051.

PERFORMANCE

The following tables give a survey about the Core area and performance in Programmable Logic Devices after Place & Route (CPU features and peripherals have been included):

Device	Speed grade	cpuclk F_{max}	utmiclk F_{max}
CYCLONE-II	-6	60 MHz	>100 MHz
CYCLONE-III	-6	70 MHz	>100 MHz
STRATIX-II	-3	100 MHz	>100 MHz
STRATIX-III	-2	110 MHz	>100 MHz
Arria GX	-6	80 MHz	>100 MHz

Core performance in ALTERA® devices

Area utilized by complete, integrated USB 2.0 HID Design Platform in vendor specific technologies are summarized in table below.

Component	Area [LC]	[FFs]
CPU interface	270	170
UTMI interface	310	230
SRAM interface	130	95
EP0 endpoint	180	140
EP1 endpoint	190	155
DP8051XP CPU	1220	320
DoCD™ debug IP core	450	270
Total area	2750	1380

Core components area utilization in STRATIX-II, STRATIX-III and Arria GX families

Component	Area [LC]	[FFs]
CPU interface	390	170
UTMI interface	450	230
SRAM interface	190	95
EP0 endpoint	260	140
EP1 endpoint	300	155
DP8051XP CPU	1850	320
DoCD™ debug IP core	600	270
Total area	4040	1380

Core components area utilization in CYCLONE-II and CYCLONE-III families

CONTACT

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