

# DI2CSB

## I<sup>2</sup>C Bus Interface Slave - Base version

### ver 3.00

#### OVERVIEW

I<sup>2</sup>C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data transmission over a short distance between many devices. The DI2CSB provides an interface between a passive target device e.g. memory, LCD display, pressure sensors etc. and an I<sup>2</sup>C bus. It can work as a slave receiver or transmitter depending on working mode determined by a master device. Very simple interface, composed with the read, write and data signals, allows easy connection to the target devices. The core doesn't require programming and is ready to work after power up/reset. The read, write, burst read, burst write and repeated start transmissions are automatically recognized by the core. The core incorporates all features required by I<sup>2</sup>C specification. The DI2CSB supports the following transmission modes: Standard, Fast and High Speed.

#### KEY FEATURES

- Conforms to v.3.0 of the I<sup>2</sup>C specification
- Slave operation
  - *Slave transmitter*
  - *Slave receiver*
- Supports 3 transmission speed modes
  - *Standard (up to 100 kb/s)*
  - *Fast (up to 400 kb/s)*
  - *Fast Plus (up to 1 Mb/s)*
  - *High Speed (up to 3,4 Mb/s)*
- Allows operation from a wide range of input clock frequencies
- Support for reads, writes, burst reads, burst writes, and repeated start
- 7-bit addressing

- No programming required
- Simple interface allows easy connection to target device e.g. memory, LCD display, pressure sensors etc.
- Fully synthesizable
- Static synchronous design with positive edge clocking and synchronous reset
- No internal tri-states
- Scan test ready

#### APPLICATIONS

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio
- Low-power applications
- Communication systems
- Cost-effective reliable automotive systems

#### DELIVERABLES

- ◆ Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF netlist
- ◆ VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- ◆ Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes

- Delivery the documentation updates
- Phone & email support

## LICENSING

Comprehensible and clearly defined licensing methods without royalty per chip fees make using of IP Core easy and simply.

Single Site license option is dedicated for small and middle sized companies making its business in one place.

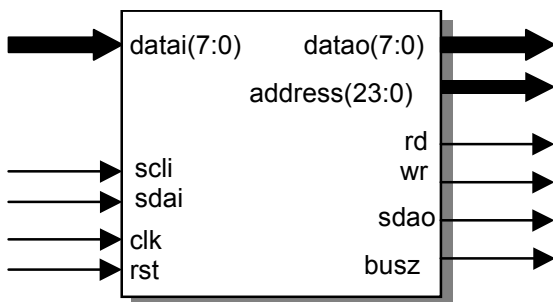
Multi Sites license option is dedicated for corporate customers making its business in several places. Licensed product can be used in selected branches of corporate.

In all cases number of IP Core instantiations within a project, and number of manufactured chips are unlimited. The license is royalty per chip free. There is no time of use restrictions.

There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

## SYMBOL



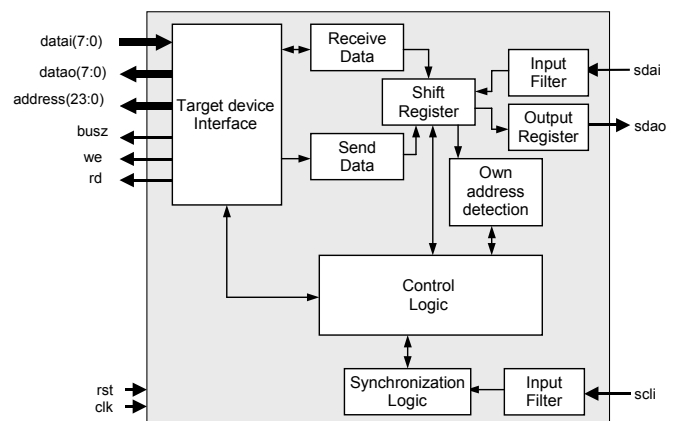
## PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
datai(7:0)	input	Data bus from target device
scli	input	I <sup>2</sup> C bus clock line (input)
sdai	input	I <sup>2</sup> C bus data line (input)
datao(7:0)	output	Data bus to target device
address(23:0)	output	Address of accessed register
busz	output	Turns datao into Z state
wr	output	Write strobe for target device
rd	output	Read strobe for target device
sdao	output	I <sup>2</sup> C bus data line (output)

## BLOCK DIAGRAM

Figure below shows the DI2CSB IP Core block diagram.

**Target device Interface** – Performs the interface functions between DI2CSB internal blocks and target device. Allows easy connection of the core to a passive devices e.g. memory, LCD display, pressure sensors, I/O devices etc.



**Control Logic** – Manages execution of all commands sent via interface. Synchronizes internal data flow.

**Shift Register** – Controls SDA line, performs data and address shifts during the data transmission and reception.

**Input Filter** – Performs spike filtering.

**Synchronization Logic** – Synchronizes data and address shifts during the data transmission and reception. SCLI spikes are filtered by this unit.

## PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route (all key features have been included):

Device	Speed grade	Logic Cells	F <sub>max</sub>
MERCURY	-5	95	220 MHz
STRATIX	-5	95	230 MHz
CYCLONE	-6	95	195 MHz
APEX II	-7	95	220 MHz
APEX20KC	-7	95	170 MHz
APEX20KE	-1	95	130 MHz
APEX20K	-1	95	94 MHz
ACEX1K	-1	95	99 MHz
FLEX10KE	-1	95	95 MHz
MAX 7000AE	-4	50	107 MHz
MAX 3000A	-4	50	107 MHz
MAX II	-3	75	154 MHz

*Core performance in ALTERA® devices*



The main features of each Digital Core Design I<sup>2</sup>C compliant cores have been summarized in table below. It gives a briefly member characterization helping user to select the most suitable IP Core for its application.

Design	I <sup>2</sup> C specification version	Master operation	Slave operation	CPU interface	Passive device interface	Interrupt generation	Clock synchronization	Arbitration	7-bit addressing	10-bit addressing	Standard mode	Fast mode	Fast Plus mode	High-speed mode	User defined timing	Spike filtering
DI2CM	3.0	✓	-	✓	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
DI2CS	3.0	-	✓	✓	-	✓	✓	-	✓	-	✓	✓	✓	✓	✓	✓
DI2CSB	3.0	-	✓	-	✓	-	-	-	✓	-	✓	✓	✓	✓	-	✓
DI2CMS	3.0	✓	✓	✓	-	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

*I<sup>2</sup>C cores summary table*

## CONTACTS

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