

DLIN

LIN Bus Controller

v. 1.03

OVERVIEW

The DLIN is a soft core of the Local Interconnect Network (LIN) bus controller, which provides single master with multiple slaves communication concept. The LIN is a serial communication protocol, primarily designed to be used in automotive application. Compared to CAN, LIN is slower, but is simpler and more cost effective. It's used in applications, where events happen in "human time". It is ideal for communication in intelligent sensors and actuators, where the bandwidth and versatility of CAN, is not required. DLIN core provides an interface between a microprocessor/microcontroller and LIN bus. It can work as a master or slave LIN mode, depending on work mode, determined by microprocessor/microcontroller. The DLIN controller supports transmission speed between 1kb/s and 20kb/s and can transmit and receive LIN messages compatible to LIN 1.3 and LIN 2.1. Reported status information includes the type and condition of transfer operations, being performed by the DLIN, as well as wide range of LIN error conditions (overrun, framing, parity, timeout). The DLIN includes programmable timer, which allows detection of timeout and synchronization error. The core is discribed at RTL level, allowing target use in FPGA and ASIC technologies.

KEY FEATURES

- Conforms with LIN 2.1 and LIN 1.3 specification
- Automatic LIN Header handling
- Automatic Re-synchronization
- Data rate between 1Kbit/s and 20 Kbit/s
- Master and Slave work modes
- Time-out detection

- Extended error detection
- "Break-in-data" support

APPLICATIONS

- Automotive, industrial
- Embedded communication systems

DELIVERABLES

- ◆ Source code:
 - VHDL Source Code
 - VERILOG Source Code
- ◆ VHDL & VERILOG test bench environment
 - Active-HDL automatic simulation macros
 - ModelSim automatic simulation macros
 - NCSim automatic simulation macros
 - Tests with reference responses
- ◆ Technical documentation
 - Installation notes
 - HDL core specification
 - Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - IP Core implementation support
 - 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods, without royalty-per-chip fees, make using of IP Core easy and simple.

Single Site license option – it is dedicated for small and middle sized companies, running their business at one location.

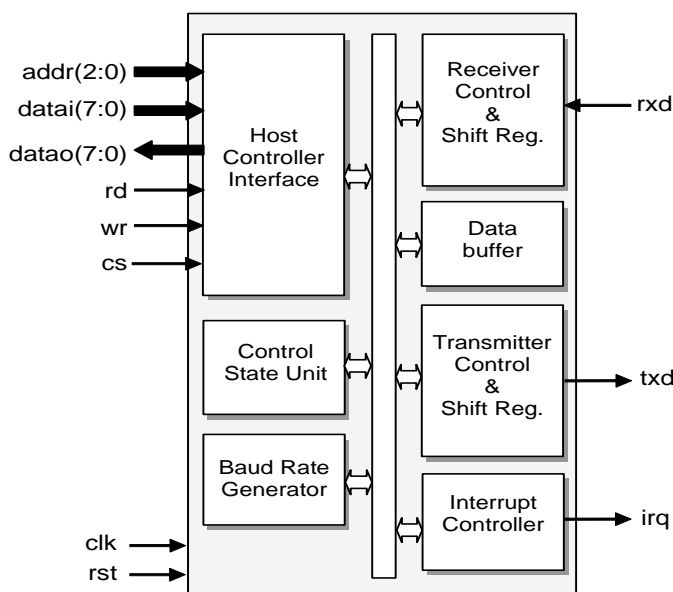
Multi Sites license option – it is dedicated for corporate customers, running their business at several places. Licensed product can be used in selected company branches. In all cases, number of IP Core instantiation within a project and number of manufactured chips are unlimited. The license is royalty-per-chip free. There is no restrictions regarding the time of use.

There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

BLOCK DIAGRAM

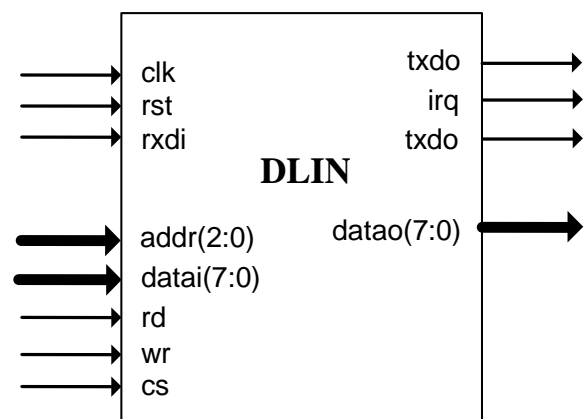
The figure below shows the DLIN IP Core block diagram.



PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
cs	input	Chip select
rd	input	Read data strobe
wr	input	Write data strobe
addr(2:0)	input	Address bus
datai(7:0)	input	Host output data bus
rxdo	input	LIN receive data
datao(7:0)	output	Input data bus
irq	output	Interrupt signal
txdo	output	LIN transmit data

SYMBOL



Host Controller Interface – accepts inputs from the system bus and generates control signals for other DLIN functional blocks. Address bus ADDR(2:0), selects one of register to be read from/written into. Active level of RD, WR and CS, can be configurable. RD and WR are ignored, unless the DLIN has been selected, by activating CS input.

Control State Unit– is composed of two state machines, the master and the slave, which control master and slave tasks. The master task handles all bus communication. It must initiate any slave response, by sending out a synch break, a synch field and protected identifier field. Slave task is respon-



sible for sending the response message, if it is addressed by the master.

Baud Rate Generator – The DLIN contains a programmable 15 bit baud generator, which divides clock input, by a divisor in the range between 1 and (2¹⁵-1). The output frequency of the baud generator is 32 x the baud rate. The formula for the divisor is:

$$BR = \frac{f}{(32 \cdot Divisor)}$$

Two registers, called divisor latches DLL and DLH, store the divisor in the 15-bit binary format.

Receiver Control & Shift Register – is responsible for receiving frame from LIN bus. Provides necessary function for data reception, frame timing and error checking.

Data Buffer – stores the receive or transmit data.

Transmitter Control & Shift Register – Performs transmit management function, sends data by LIN bus

Interrupt Controller – Interrupt controller works with transmitter, receiver and control unit, to indicate DLIN transmission events or errors. User can configure, which events may generate interrupt by enabled or disabled corresponding bits, in Interrupt Enable register. When interrupt is generated, host can find information about reason by reading LIN Status Register.

PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route (all key features have been included):

Device	Speed grade	Logic Cells	F _{max}
CYCLONE	-6	674	159
CYCLONE2	-6	670	207
STRATIX	-5	674	147
STRATIX2	-3	467	266
STRATIXGX	-5	462	184
APEX II	-7	730	117
APEX20KC	-7	730	115
APEX20KE	-1	730	98
ACEX1K	-1	773	85
FLEX10KE	-1	773	85

Core performance in ALTERA® devices



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