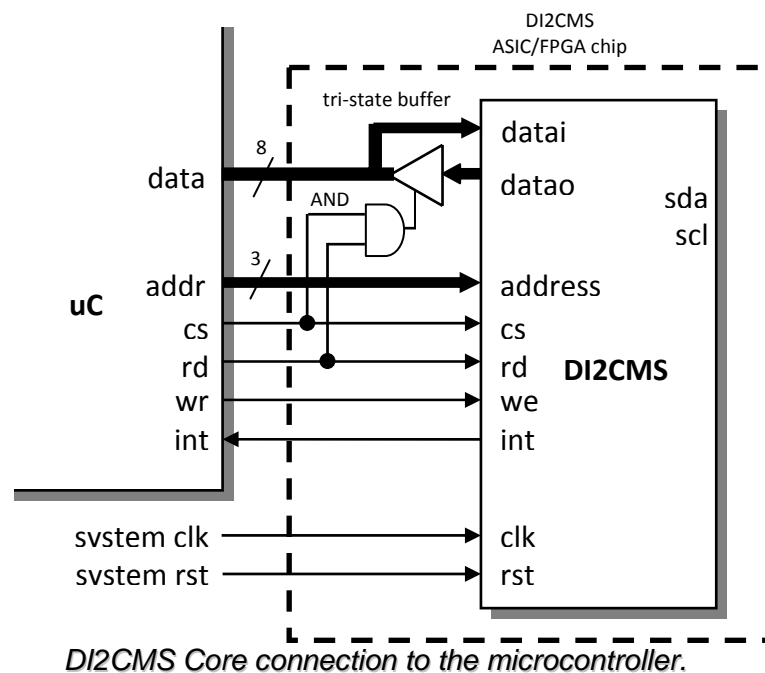


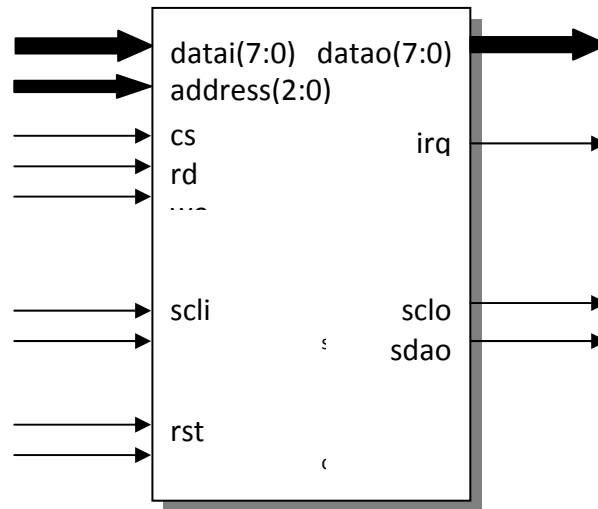
Connection DI2CMS I2C Master/Slave Core to microcontroller and I2C bus

This document describe how to connect the DI2CMS I2C Master/Slave device to the microcontroller with separated address/data buses.



The data output bus of the DI2CMS Core “dataao” is connected to the bi-directional microcontroller data bus via a tri-state buffer. Data on the DI2CMS “dataao” bus appears only during reading the DI2CMS contents (cs and rd pins controls the tri-state buffer) by the microcontroller. In any other cases the DI2CMS “dataao” bus is driven into high-impedance.

The DI2CMS core contains both DI2CM and DI2CS cores connected together as single Master/Slave I2C controller. DI2CMS pinout is shown below.



PIN	TYPE	ACTIVE	DESCRIPTION
clk	input	-	Global clock
rst	input	high	Global reset
address(2:0)	input	-	Processor address lines
cs	input	high	Chip select
we	input	high	Processor write strobe
rd	input	high	Processor read strobe
scli	input	-	I ² C bus clock line (input)
sdai	input	-	I ² C bus data line (input)
datai(7:0)	input	-	Processor data bus (input)
datao(7:0)	output	-	Processor data bus (output)
sclo	output	-	I ² C bus clock line (output)
sdao	output	-	I ² C bus data line (output)
irq	output	high	Processor interrupt line

DI2CMS pins description

There are seven DI2CMS Master/Slave registers used to interface to the host. They are listed below.

Register	Address
Master Slave address	000
Master Control	001
Master Transmitted data	010
Master Timer period*	011
Slave Own Address	100
Slave Control	101
Slave Transmitted data	110

*double register, refer to the section below

Registers for writing

Register	Address
Master Slave address	000
Master Status	001
Master Received data	010
Master Timer period*	011
Slave Own Address	100
Slave Status	101
Slave Received data	110

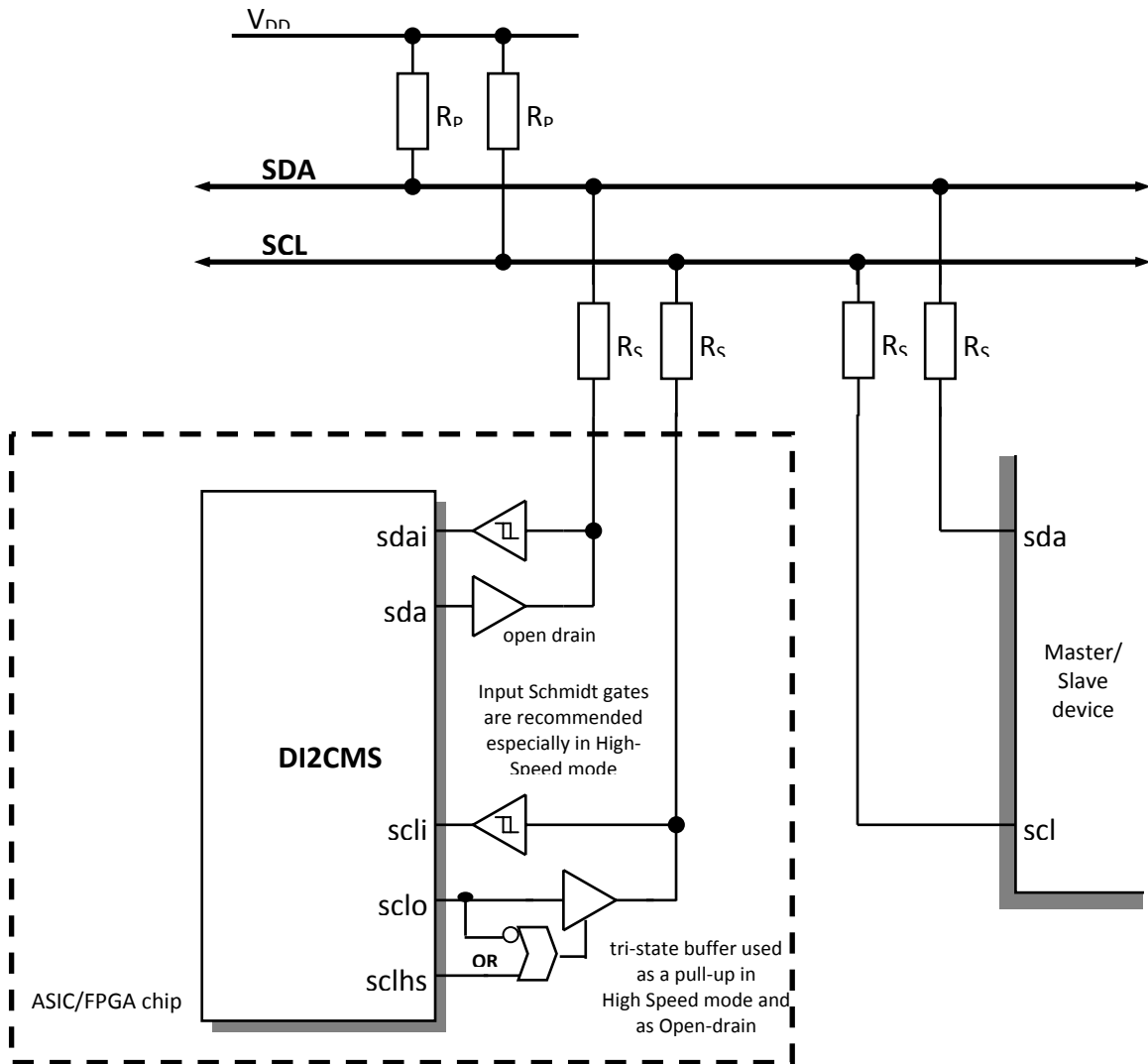
*the only STANDARD,FAST I2CTP value can be read, refer to the section below

Registers for reading

For more details about DI2CMS please refer to DI2CM and DI2CS specification.

Application note v4.04

Figure below shows connection of DI2CMS Core into global I2C Bus in systems operating in I2C Standard/Fast mode as well as in I2C High Speed Mode.



Input Schmitt gates are recommended especially in High-Speed I2C mode. They prevent incidental erroneous behavior caused by slow rising edges on input SCL and SDA lines.