

## DSPI data transfer formats

During a SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line synchronizes shifting and sampling of the information on the two serial data lines: MISO (master in – slave out) and MOSI (master out - slave in). A slave select (SS) line allows individual selection of a SPI slave device; slave devices that are not selected do not interfere with SPI bus activities. On a master SPI device, the slave select line can optionally be used to indicate a multiple-master bus contention. The SPI bus allows configure the polarity (CPOL) and phase (CPHA) of MISO and MOSI lines. These two parameters allow four different transferred data formats.

Figures below show a timing diagrams of an SPI transfer where CPHA is 0 and 1. Two waveforms are shown for SCK: one for CPOL equals 0 and another for CPOL equals 1. The diagram may be interpreted as a master or slave timing diagram since the SCK, master in/slave out (MISO), and master out/slave in (MOSI) pins are directly connected between the master and the slave. The MISO signal is the output from the slave, and the MOSI signal is the output from the master. The SS line is the slave select input to the slave; the SS pin of the master is not shown but is assumed to be inactive. The SS pin of the master must be high. This timing diagram functionally depicts how a transfer takes place; it should not be used as a replacement for data-sheet parametric information.

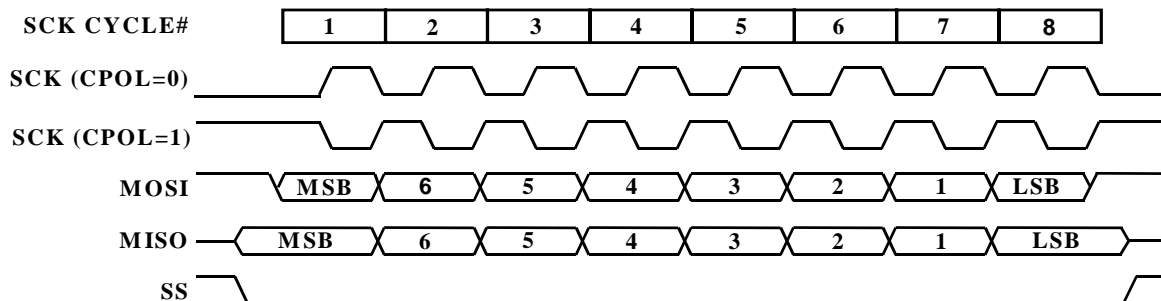


Figure 1. CPHA Equals Zero SPI Transfer Format

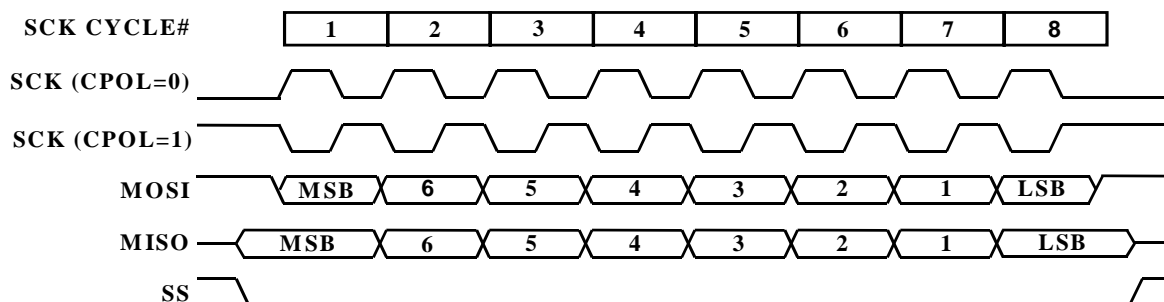


Figure 2. CPHA Equals One SPI Transfer Format

**Application note v4.04**

When  $CPHA = 0$ , the SS line must be deasserted and reasserted between each successive serial byte. Also, if the slave writes data to the SPI data register (SPDR) while SS is active low, a write-collision error results. When  $CPHA = 1$ , the SS line may remain active low between successive transfers (can be tied low at all times). This format is sometimes preferred in systems having a single fixed master and a single slave driving the MISO data line.