

DCORDIC

CORDIC processor

v. 1.16

OVERVIEW

The DCORDIC uses the **CORDIC** algorithm, to compute **trigonometric**, reverse trigonometric, **hyperbolic** and reverse hyperbolic functions. It supports sine, cosine and arctangent functions for hyperbolic and trigonometric systems. Logarithm, square root and exponent functions can also be computed. It supports fixed point 24-bit numbers.

OPERATING MODES

- Trigonometric system
- Hyperbolic system
- Rotation mode
- Vectoring mode

APPLICATIONS

- DSP algorithms
- Digital filtering
- Math coprocessors

KEY FEATURES

- 24-bit precision (IEEE-754 single precision real mantissa format)
- 4-ulp accuracy (34-bit internal registers)
- Fully configurable
- Performs the following functions:
 - $\sin(\theta)$, $\cos(\theta)$
 - $\sinh(\theta)$, $\cosh(\theta)$
 - $\arctan(x)$
 - $\operatorname{arctanh}(x)$
 - $\ln(x)$, e^x , \sqrt{x}

DELIVERABLES

- ◆ Source code:
 - VHDL Source Code or/and
 - VERILOG Source Code or/and
 - Encrypted, or plain text EDIF netlist
- ◆ VHDL & VERILOG test bench environment
 - Active-HDL automatic simulation macros
 - ModelSim automatic simulation macros
 - Tests with reference responses
- ◆ Technical documentation
 - Installation notes
 - HDL core specification
 - Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - IP Core implementation support
 - 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods, without royalty-per-chip fees, make using of IP Core easy and simple.

Single Site license option – it is dedicated for small and middle sized companies, running their business at one location.

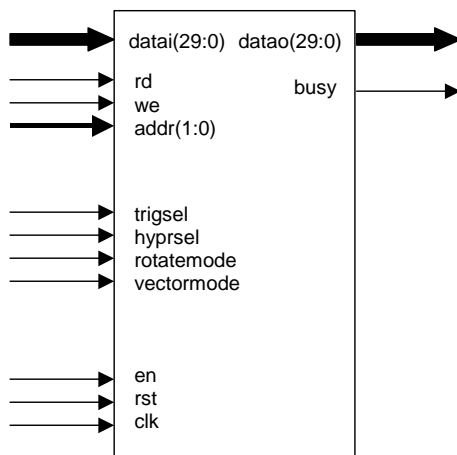
Multi Sites license option – it is dedicated for corporate customers, running their business at several places. Licensed product can be used in selected company branches.

In all cases, number of IP Core instantiation within a project and number of manufactured chips are unlimited. The license is royalty-per-chip free. There is no restrictions regarding the time of use.

There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

SYMBOL



PINS DESCRIPTION

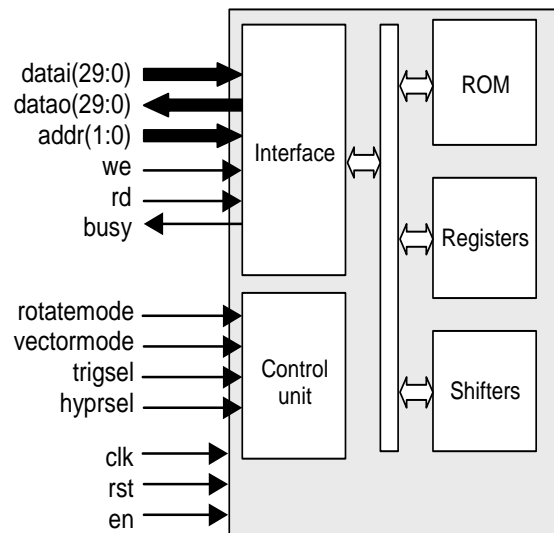
PIN	TYPE	DESCRIPTION
clk	Input	Global clock
rst	Input	Global reset
en	Input	Enable computing
datai[29:0]	Input	Data bus (input)
we	Input	Write data into register
rd	Input	Read data from register
cs	Input	Chip select
addr[1:0]	Input	Select register to read/write
rotatemode	Input	Rotate mode select
vectormode	Input	Vectoring mode select
hyprsel	Input	Hyperbolic system select
trigsel	Input	Trigonometric system select
datao[29:0]	Output	Data bus (output)
busy	Output	Busy indicator

BLOCK DIAGRAM

ROM – stores constant coefficients used for hyperbolic and trigonometric operations.

Registers – contains all data registers, holds temporary operation results, as well as final results. Input arguments are also written to this register.

Control Unit – maintains control operation on *Registers* module, *Shifters* module and *ROM* unit, while busy is active.



Shifters – performs shifting operations in successful iterations. Number of shifts vary and depend on internal iteration cycle and computed functions.

Interface – performs communication between internal CORDIC modules and external devices. Signalizes when output registers contain a valid result.



CONTACT

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