

DP80C51

Pipelined High Performance

8-bit Microcontroller

v. 4.01

OVERVIEW

DP80C51 is an **ultra high performance, speed optimized** soft core, of a single-chip 8-bit embedded controller, dedicated to operate with **fast** (typically on-chip) and **slow** (off-chip) **memories**. The core has been designed with a special concern for **performance to power consumption** ratio. This ratio is extended by an advanced power management unit **PMU**. DP80C51 soft core is 100% binary and **pin compatible** with the industry standard 8051 8-bit microcontroller. There are two configurations of the DP80C51: **Harvard**, where external data and program buses are separated and **von Neumann**, with common program and external data bus. DP80C51 has Pipelined RISC architecture, up to **10 times faster**, compared to standard architecture -it executes **85-200 million instructions** per second. This performance can also be exploited to great advantage in **low power** applications, where the core can be clocked over ten times more slowly, than the original implementation, for no performance penalty. DP80C51 is delivered with **fully automated testbench** and **complete set of tests**, allowing easy package validation, at each stage of SoC design flow.

CPU FEATURES

- 100% pin compatible with industry 8051 standard
- 100% software compatible with 8051 industry standard
- Pipelined RISC architecture enables to execute instructions up to 10 times faster, compared to standard 8051
- 24 times faster multiplication
- 12 times faster addition

- Up to 256 bytes of internal (on-chip) Data Memory
- Up to 64K bytes of internal (on-chip) or external (off-chip) Program Memory
- User programmable Program Memory Wait States solution, for wide range of memories speed
- User programmable External Data Memory Wait States solution for, wide range of memories speed
- Dedicated signal for Program Memory writes.
- Interface for additional Special Function Registers
- Fully synthesizable, static synchronous design, with positive edge clocking and no internal tri-states
- Scan test ready
- **2.0 GHz virtual** clock frequency in a 0.25u technological process

PERIPHERALS

- **DoCD™** debug unit
 - *Processor execution control*
 - *Run*
 - *Halt*
 - *Step into instruction*
 - *Skip instruction*
 - *Read-write all processor contents*
 - *Program Counter (PC)*
 - *Program Memory*
 - *Internal (direct) Data Memory*
 - *Special Function Registers (SFRs)*
 - *External Data Memory*
 - *Code execution breakpoints*
 - *one real-time PC breakpoint*
 - *unlimited number of real-time OPCODE breakpoints*

- *Hardware execution watch-point*
 - *one at Internal (direct) Data Memory*
 - *one at Special Function Registers (SFRs)*
 - *one at External Data Memory*
- *Hardware watch-points activated at a certain*
 - *address by any write into memory*
 - *address by any read from memory*
 - *address by write into memory a required data*
 - *address by read from memory a required data*
- *Unlimited number of software watch-points*
 - *Internal (direct) Data Memory*
 - *Special Function Registers (SFRs)*
 - *External Data Memory*
- *Unlimited number of software breakpoints*
 - *Program Memory(PC)*
- *Automatic adjustment of debug data transfer speed rate between HAD and Silicon*
- *JTAG Communication interface*
- **Power Management Unit**
 - *Power management mode*
 - *Switchback feature*
 - *Stop mode*
- **Interrupt Controller**
 - *2 priority levels*
 - *2 external interrupt sources*
 - *3 interrupt sources from peripherals*
- **Four 8-bit I/O Ports**
 - *Bit addressable data direction for each line*
 - *Read/write of single line and 8-bit group*
- **Two 16-bit timer/counters**
 - *Timers clocked by internal source*
 - *Auto reload 8-bit timers*
 - *Externally gated event counters*
- **Full-duplex serial port**
 - *Synchronous mode, fixed baud rate*
 - *8-bit asynchronous mode, fixed baud rate*
 - *9-bit asynchronous mode, fixed baud rate*
 - *9-bit asynchronous mode, variable baud rate*

CONFIGURATION

The following parameters of the DP80C51 core can be easily adjusted to requirements of dedicated application and technology. Configuration of the core can be effortlessly done, by changing appropriate constants in the package file. There is no need to change any parts of the code.

- Internal Program Memory - synchronous

- type - asynchronous
- Internal Program ROM - 0 - 64kB
 - Memory size -
- Internal Program RAM - 0 - 64kB
 - Memory size -
- Interrupts - subroutines
 - location -
- Power Management Mode - used
 - unused
- Stop mode - used
 - unused
- DoCD™ debug unit - used
 - unused

Besides parameters mentioned above, all available peripherals and external interrupts can be excluded from the core, by changing appropriate constants in the package file.

DELIVERABLES

- ◆ Source code:
 - VHDL Source Code or/and
 - VERILOG Source Code or/and
 - Encrypted, or plain text EDIF netlist
- ◆ VHDL & VERILOG test bench environment
 - NCSim automatic simulation macros
 - ModelSim automatic simulation macros
 - Active-HDL automatic simulation macros
 - Tests with reference responses
- ◆ Technical documentation
 - Installation notes
 - HDL core specification
 - Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - IP Core implementation support
 - 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods, without royalty-per-chip fees, make using of IP Core easy and simple.

Single Site license option – it is dedicated for small and middle sized companies, running their business at one location.

Multi Sites license option – it is dedicated for corporate customers, running their business at several places. Licensed product can be used in selected company branches. In all cases, number of IP Core instantiation within a project and number of manufactured chips are unlimited. The license is royalty-per-chip free. There is no restrictions regarding the time of use.

There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

DESIGN FEATURES

◆ PROGRAM MEMORY:

The DP80C51 soft core is dedicated to operate with Internal and External Program Memory. Internal Program Memory can be implemented as:

- ROM located in address range between $0x0000 \div (ROM_{size}-1)$
- RAM located in address range between $(RAM_{size}-1) \div 0xFFFF$

External Program Memory can be implemented as ROM or RAM located in address range between $ROM_{size} \div RAM_{size}$.

◆ INTERNAL DATA MEMORY:

The DP80C51 can address Internal Data Memory of up to 256 bytes. The Internal Data Memory can be implemented, as a Single-Port synchronous RAM.

◆ EXTERNAL DATA MEMORY:

The DP80C51 soft core can address up to 64 kB of External Data Memory.

◆ USER SPECIAL FUNCTION REGISTERS:

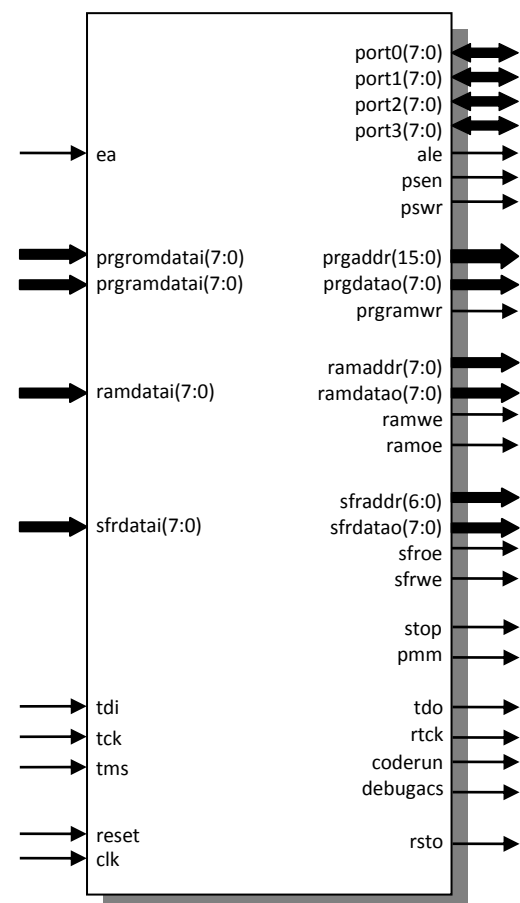
Up to 104 External (user) Special Function Registers (ESFRs) may be added to the DP80C51 design. ESFRs are memory mapped into Direct Memory, between addresses 0x80 and 0xFF, in the same manner, as core SFRs. They may

occupy any address, that is not occupied by a SFR core.

◆ WAIT STATES SUPPORT:

The DP80C51 soft core is dedicated for operation with a wide range of Program and Data memories. Slow Program and External Data memory, may assert a memory WAIT signal, to hold up CPU activity for required period of time.

SYMBOL



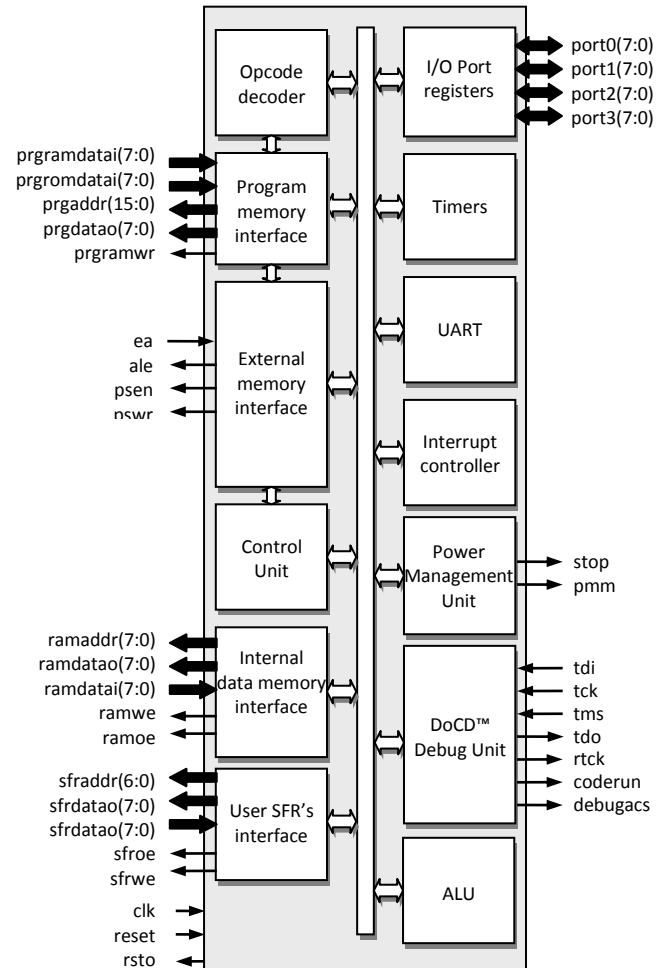
PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
reset	input	Global reset input
port0[7:0]	bidir	I/O Port 0, multifunctional Data/LSB address of external memory
port1[7:0]	bidir	I/O Port 1
port2[7:0]	bidir	I/O Port 2, multifunctional

PIN	TYPE	DESCRIPTION
		MSB address of external memory
port3[0]	bidir	I/O Port 3.0 Serial receiver input/output port
port3[1]	bidir	I/O Port 3.1 Serial transmitter output port
port3[2]	bidir	I/O Port 3.2, multifunctional Interrupt 0 input/timer 0 gate
port3[3]	bidir	I/O Port 3.3, multifunctional Interrupt 1 input/timer 1 gate
port3[4]	bidir	I/O Port 3.4, multifunctional Timer 0 external clock line
port3[5]	bidir	I/O Port 3.5, multifunctional Timer 1 external clock line
port3[6]	bidir	I/O Port 3.6 External Data Memory write
port3[7]	bidir	I/O Port 3.7 External Data Memory read
ea	input	Enable all external program memory
prgramdatai[7:0]	input	Data bus from int. RAM prog. memory
prgromdatai[7:0]	input	Data bus from int. ROM prog. memory
ramdatai[7:0]	input	Data bus from internal data memory
sfrdatai[7:0]	input	Data bus from user SFR's
tdi	input	DoCD™ TAP data input
tck	input	DoCD™ TAP clock input
tms	input	DoCD™ TAP mode select input
rsto	output	Reset output
prgaddr[15:0]	output	Internal program memory address bus
prgdatao[7:0]	output	Data bus for internal program memory
prgramwr	output	Internal program memory write
ale	output	Address Latch Enable
psen	output	Program Store (memory) read Enable
pswr	output	Program Store (memory) Write
ramaddr[7:0]	output	Internal Data Memory address bus
ramdatao[7:0]	output	Data bus for internal data memory
ramoe	output	Internal data memory output enable
ramwe	output	Internal data memory write enable
sfraddr[6:0]	output	Address bus for user SFR's
sfrdatao[7:0]	output	Data bus for user SFR's
sfroe	output	User SFR's read enable
sfrwe	output	User SFR's write enable
tdo	output	DoCD™ TAP data output
rtck	output	DoCD™ return clock line
debugacs	output	DoCD™ accessing data
coderun	output	CPU is executing an instruction
pmm	output	Power management mode indicator

PIN	TYPE	DESCRIPTION
stop	output	Stop mode indicator

BLOCK DIAGRAM



UNITS SUMMARY

Arithmetic Logic Unit - performs the arithmetic and logic operations, during execution of an instruction. It contains accumulator (ACC), Program Status Word (PSW), (B) registers and related logic, like arithmetic unit, logic unit, multiplier and divider.

Opcode Decoder - Performs an opcode decoding instruction and control functions for all other blocks.

Control Unit - Performs the core synchronization and data flow control. This module is directly con-



nected to Opcode Decoder and manages execution of all microcontroller tasks.

Program Memory Interface – Program Memory Interface contains Program Counter (PC) and related logic. It performs the instructions code fetching. Program Memory can be also written. This feature allows usage of a small boot loader, to load new program into ROM, RAM, EPROM or FLASH EEPROM storage via UART, SPI, I2C or DoCD™ module.

External Memory Interface - Contains memory access related registers, such as Data Page High (DPH), Data Page Low (DPL). It performs the external Program and Data Memory addressing and data transfers. Program fetch cycle length can be programmed by the user. This feature is called Program Memory Wait States, and it allows core to work with different speed program memories.

Internal Data Memory Interface – Interface controls access into the internal memory of size up to 256 bytes. It contains 8-bit Stack Pointer (SP) register and related logic.

User SFRs Interface – Special Function Registers interface controls access to the special registers. It contains standard and used defined registers and related logic. User defined external devices can be quickly accessed (read, written, modified), by using all direct addressing mode instructions.

Interrupt Controller – Interrupt control module is responsible for the interrupt manage system, for the external and internal interrupt sources. It contains interrupt related registers, such as Interrupt Enable (IE), Interrupt Priority (IP) and (TCON) registers. Please note, that external pins of this module are connected to appropriate pins of P3 port.

Timers – System timers module. Contains two 16 bits configurable timers: Timer 0 (TH0, TL0), Timer 1 (TH1, TL1) and Timers Mode (TMOD) registers. In the timer mode, timer registers are incremented every 12 CLK periods, when appropriate timer is enabled. In the counter mode, the timer registers are incremented every falling transition on their corresponding input pins (T0, T1), if gates are opened (GATE0, GATE1). T0, T1 input pins are

sampled every CLK period. It can be used as a clock source for UARTs. Please note, that external pins of this module are connected to appropriate pins of P3 port.

UART0 – Universal Asynchronous Receiver and Transmitter module is full duplex, which means, that it can transmit and receive concurrently. Includes Serial Configuration register (SCON), serial receiver and transmitter buffer (SBUF) registers. Its receiver is double-buffered, meaning, it can commence reception of a second byte, before the previously received byte has been read from the receive register. Writing to SBUF0 loads the transmit register and reading SBUF0, reads a physically separate receive register. Works in 3 asynchronous and 1 synchronous modes. UART0 can be synchronized by Timer 1. Please note, that external pins of this module are connected to appropriate pins of P3 port.

Ports - Block contains 8051's general purpose I/O ports. Each of port's pin can be read/written as a single bit or as a 8-bit bus P0, P1, P2, P3. The P0, P2, P3 are multi-functional ports. When used with External memory P0 works as a multiplexed Data/LSB address to memory, and P2 works as a MSB address to external memory, P3.6 is a write signal and P3.7 is a read signal. Functionality of port is the same as in legacy 80C51 microcontroller.

Power Management Unit – Power Management Unit contains advanced power saving mechanisms with switchback feature, allowing external clock control logic to stop clocking (Stop mode) or run core in lower clock frequency (Power Management Mode), to significantly reduce power consumption. Switchback feature allows UARTs and interrupts to be processed in full speed mode, if enabled. It is highly desirable, when microcontroller is planned to be used in portable and power critical applications.

DoCD™ Debug Unit – It is a **real-time hardware debugger**, which provides debugging capability of a whole SoC system. Unlike other on-chip debuggers, DoCD™ ensures **non-intrusive debugging** of running application. It can halt, run, step into or skip an instruction, read/write any contents of

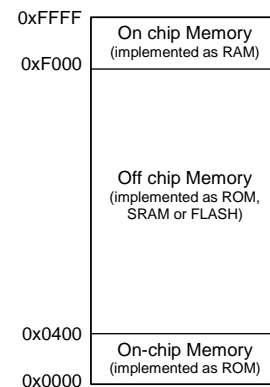


microcontroller, including all registers, internal and external program memories and all SFRs, including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware watchpoints can be set and controlled on internal and external data memories and also on SFRs. Hardware watchpoints are executed, if any write/read occurs at particular address, with certain data pattern or without pattern. Two additional pins: CODERUN and DE-BUGACS, indicate the state of the debugger and CPU. CODERUN is active, when CPU is executing an instruction. DEBUGACS pin is active, when any access is performed by DoCD™ debugger. The DoCD™ system includes JTAG interface and complete set of tools, to communicate and work with core in real time debugging. It is built, as a scalable unit and some features can be turned off, to save silicon and reduce power consumption. When debugger is not used, it is automatically switched to power save mode. Finally, when debug option is no longer used, whole debugger is turned off.

PROGRAM CODE SPACE IMPLEMENTATION

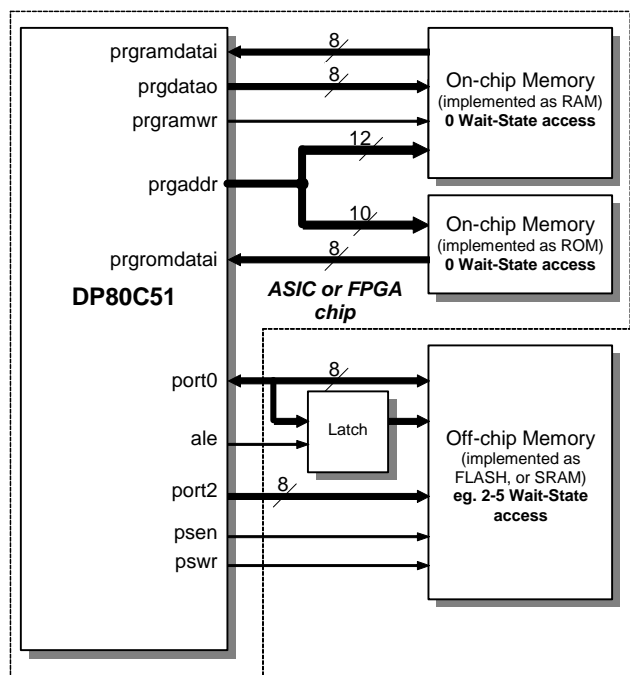
The figure on the right, shows an example Program Memory space implementation in systems with DP80C51 Microcontroller core. The On-chip Program Memory located in address space, between 0kB and 1kB, is typically used for BOOT code, with system initialization functions. This part of the code is typically implemented as ROM. The on-chip Program Memory, located in address space between 60kB and 64kB, is typically used for timing critical part of the code e.g. interrupt subroutines, arithmetic functions etc. This part of the code is typically implemented as RAM and can be loaded by the BOOT code during initialization phase, from off-chip memory or through RS232 interface, from external device. From the two spaces mentioned above, the program code is executed without wait-states and can achieve a top performance, up to 200 million instructions per second (many instructions executed in one clock cycle). The off-chip Program Memory located in address space between 1kB and 60kB, is

typically used for main code and constants. This part of the code, is usually implemented as ROM, SRAM or FLASH device. Because of relatively long access time, the program code executed from devices mentioned above, must be fetched with additional Wait-States. Number of required Wait-States depends on memory access time and DP80C51 clock frequency.



In most cases, the proper number of Wait-States cycles is between 2-5. The READY pin can be also dynamically modulated e.g. by SDRAM controller.

The figure below shows a typical Program Memories connections in system with DP80C51 Microcontroller core.



The implementation described above, should be treated as an example. All Program Memory spaces

are fully configurable. For timing-critical applications, the whole program code can be implemented as an on-chip ROM and (or) RAM and executed without Wait-States, but for some other applications, whole program code can be implemented as a off-chip ROM or FLASH and executed with required number Wait-State cycles.

PERFORMANCE

The following tables give a survey about the Core area and performance in ASICs Devices (CPU features and peripherals have been included):

Device	Optimization	F _{max}
0.25u typical	area	100 MHz
0.25u typical	speed	250 MHz

Core performance in ASIC devices

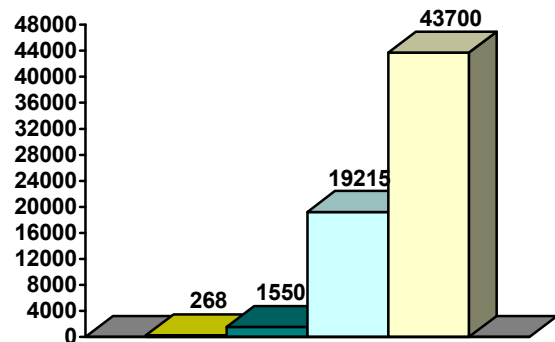
For the user, the most important factor is the application speed improvement. The most commonly used arithmetic functions and their improvement, are shown in the table below. Improvement was computed as {80C51 clock periods}, divided by {DP80C51 clock periods}, required to execute an identical function for code, executed from internal (first column) and external (second column) program memory. More details are available in the core documentation.

Function	Improvement	
8-bit addition (<i>immediate data</i>)	9,00	3,00
8-bit addition (<i>direct addressing</i>)	9,00	3,00
8-bit addition (<i>indirect addressing</i>)	9,00	3,60
8-bit addition (<i>register addressing</i>)	12,00	4,00
8-bit subtraction (<i>immediate data</i>)	9,00	3,00
8-bit subtraction (<i>direct addressing</i>)	9,00	3,00
8-bit subtraction (<i>indirect addressing</i>)	9,00	3,60
8-bit subtraction (<i>register addressing</i>)	12,00	4,00
8-bit multiplication	16,00	6,00
8-bit division	9,60	4,80
16-bit addition	12,00	4,00
16-bit subtraction	12,00	4,00
16-bit multiplication	13,60	5,47
32-bit addition	12,00	4,00
32-bit subtraction	12,00	4,00
32-bit multiplication	12,60	4,89
Average speed improvement:	11,12	4,03

Dhrystone Benchmark Version 2.1 was used, to measure Core performance. The following table gives a survey about the DP80C51 performance, in terms of Dhrystone/sec and VAX MIPS rating, for testing code executed from external (1) and internal (2) program memory.

Device	Target	Clock frequency	Dhry/sec (VAX MIPS)
80C51	-	12 MHz	268 (0.153)
80C310	-	33 MHz	1550 (0.882)
DP80C51 ¹	0.25u	250 MHz	19215 (10,938)
DP80C51 ²	0.25u	250 MHz	43700 (24.872)

Core performance in terms of Dhrystones



■ 80C51 (12MHz)
 ■ 80C310 (33MHz)
 □ DP80C51 - external program memory (250MHz)
 □ DP80C51 - internal program memory (250MHz)

Area utilized by the each unit of the DP80C51 core in vendor specific technologies, is summarized in the table below.

Component	Area	
	[Gates]	[FFs]
CPU*	6100	310
Interrupt Controller	450	40
Power Management Unit	50	5
I/O ports	400	35
Timers	550	50
UART0	650	60
Total area	8200	500

*CPU – consisted of ALU, Opcode Decoder, Control Unit, Program & Internal & External Memory Interfaces, User SFRs Interface

Core components area utilization

The main features of each DP80C51 family member have been summarized in the table below. It gives a brief member characteristic, helping you to select the most suitable IP Core for your application. You can specify your own peripheral set (including listed below and others) and requests the core modifications.

Design	Architecture speed grade	Program Memory space			Stack space size	Internal Data Memory space	External Data Memory space	External Data / Program Memory Wait States	Power Management Unit	Interface for additional SFRs	Interrupt sources	Interrupt levels	Data Pointers	Timer/Counters	UART	I/O Ports	Compare/Capture	Watchdog	Master I ² C Bus Controller	Slave I ² C Bus Controller	SPI	Fixed Point Coprocessor	Floating Point Coprocessor
		on-chip RAM	on-chip ROM	off-chip																			
DP8051CPU	10	64k	64k	64k	256	256	16M	✓	✓	✓	2	2	1	-	-	-	-	-	-	-	-	-	-
DP8051	10	64k	64k	64k	256	256	16M	✓	✓	✓	5	2	1	2	1	4	-	-	-	-	-	-	-
DP8051XP	10	64k	64k	64k	256	256	16M	✓	✓	✓	15	2	2	3	2	4	✓	✓	✓	✓	✓	✓	✓

DP8051 family of Pipelined High Performance Microcontroller Cores

The main features of each DP80390 family member have been summarized in the table below. It gives a brief member characteristic, helping you to select the most suitable IP Core for your application. You can specify your own peripheral set (including listed below and others) and requests the core modifications.

Design	Architecture speed grade	Program Memory space			Stack space size	Internal Data Memory space	External Data Memory space	External Data / Program Memory Wait States	Power Management Unit	Interface for additional SFRs	Interrupt sources	Interrupt levels	Data Pointers	Timer/Counters	UART	I/O Ports	Compare/Capture	Watchdog	Master I ² C Bus Controller	Slave I ² C Bus Controller	SPI	Fixed Point Coprocessor	Floating Point Coprocessor
		on-chip RAM	on-chip ROM	off-chip																			
DP80390CPU	10	64k	64k	8M	256	256	16M	✓	✓	✓	2	2	1	-	-	-	-	-	-	-	-	-	-
DP80390	10	64k	64k	8M	256	256	16M	✓	✓	✓	5	2	1	2	1	4	-	-	-	-	-	-	-
DP80390XP	10	64k	64k	8M	256	256	16M	✓	✓	✓	15	2	2	3	2	4	✓	✓	✓	✓	✓	✓	✓

DP80390 family of Pipelined High Performance Microcontroller Cores

CONTACT

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