

DCAN

Configurable CAN Bus Controller

ver 1.11

OVERVIEW

The DCAN is a stand-alone controller for the Controller Area Network (CAN) widely used in automotive and industrial applications. DCAN conforms to Bosch CAN 2.0B specification (2.0B Active). Core has simple CPU interface (8/16/32 bit configurable data width) with little or big endian addressing scheme. Hardware message filtering and 64 byte receive FIFO enables back-to-back message reception with minimum CPU load. The DCAN is described at RTL level allowing target use in FPGA or ASIC technologies.

FEATURES

- Conforms to Bosch CAN 2.0B Active
 - 11 and 29 bit wide message identifiers
- 8/16/32-bit CPU slave interface with little or big endianess
- Simple interface allows easy connection to CPU
- Supports both standard (11-bit identifier) and extended (29 bit identifier) frames.
- Data rate up to 1 Mbps
- Hardware message filtering (dual/single filter)
- 64 byte receive FIFO
- 16-byte transmit buffer
- No overload frames are generated
- Normal & Listen Only Mode

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- Single Shot transmission
- Ability to abort transmission
- Readable error counters
- Last Error Code
- Fully synthesizable
- Static synchronous design with positive edge clocking and synchronous reset
- No internal tri-states
- Scan test ready

DELIVERABLES

- ◆ Source code:
 - ◇ VHDL Source Code or/and
 - ◇ VERILOG Source Code or/and
 - ◇ Encrypted, or plain text EDIF netlist
- ◆ VHDL & VERILOG test bench
 - ◇ Active-HDL automatic simulation macros
 - ◇ ModelSim automatic simulation macros
 - ◇ Tests with reference responses
- ◆ Technical documentation
 - ◇ Installation notes
 - ◇ HDL core specification
 - ◇ Datasheet
- ◆ Synthesis scripts
- ◆ Example application
- ◆ Technical support
 - ◇ IP Core implementation support
 - ◇ 3 months maintenance
 - IP Core updates
 - Delivery the documentation updates
 - Phone & email support

LICENSING

Comprehensible and clearly defined licensing methods without royalty per chip fees make using of IP Core easy and simply.

Single Site license option is dedicated for small and middle sized companies making its business in one place.

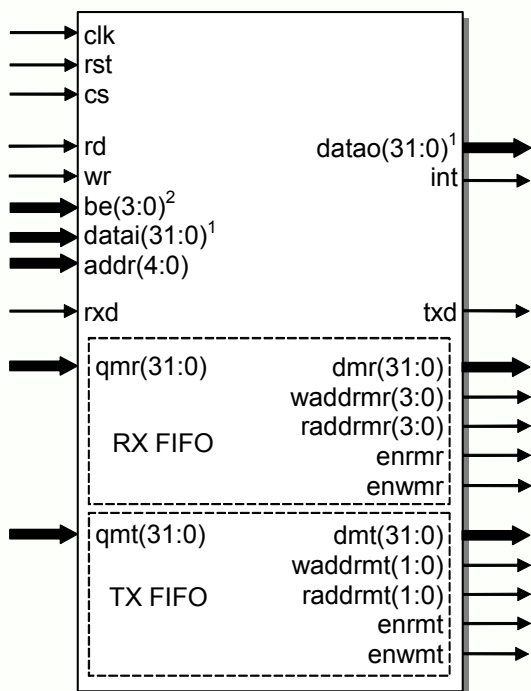
Multi Sites license option is dedicated for corporate customers making its business in several places. Licensed product can be used in selected branches of corporate.

In all cases number of IP Core instantiations within a project, and number of manufactured chips are unlimited. The license is royalty per chip free. There is no time of use restrictions.

There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

PINOUT



1 – configured data bus - 8-, 16- or 32

2 – byte enable (be) size is set accordingly to data bus size

PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
rst	input	Global reset
cs	input	Chip select
rd	input	Read data strobe
wr	input	Write data strobe
addr(4:0)	input	Host address bus
be(3:0) ²	input	Host byte enable
datai(31:0) ¹	input	Host output data bus
qmr(31:0)	input	RX DPRAM data output
qmt(31:0)	input	TX DPRAM data output
rxd	input	CAN receive data
docdbusctrl	input	DoCD debugger input
datao(31:0) ¹	output	Host input data bus
int	output	Interrupt signal
dmr(31:0)	output	RX DPRAM data input
waddrmr(3:0)	output	RX DPRAM write address
raddrmr(3:0)	output	RX DPRAM read address
enrmt	output	RX DPRAM read enable
enwmt	output	RX DPRAM write enable
dmt(31:0)	output	TX DPRAM data input
waddrmt(1:0)	output	TX DPRAM write address
raddrmt(1:0)	output	TX DPRAM read address
enrmt	output	TX DPRAM read enable
enwmt	output	TX DPRAM write enable
txd	output	CAN transmit data

BLOCK DIAGRAM

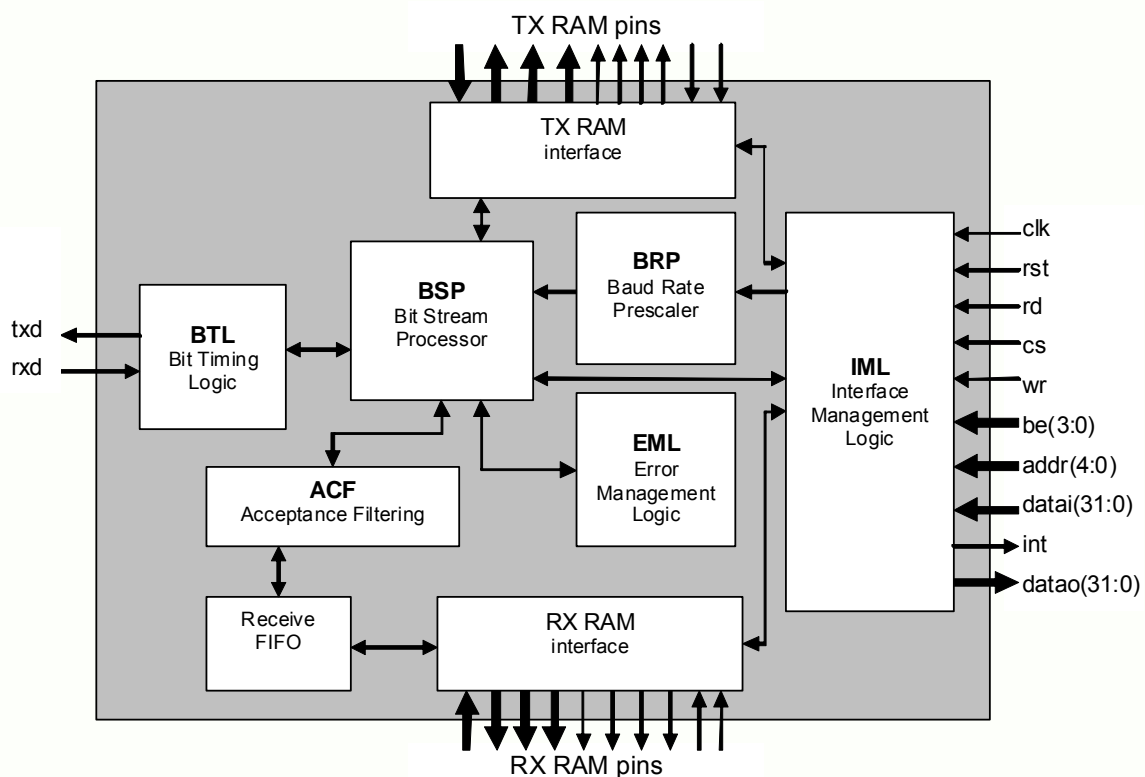
Interface Management Logic (IML) – interprets commands from the CPU, provides interrupt and status indication.

Bit Stream Processor (BSP) – translates messages into frames and vice versa.

Baud Rate Prescaler (BRP) – defines the length of time quantum.

Bit Timing Logic (BTL) – processes the bit time, calculates position of the sample point and performs synchronization.

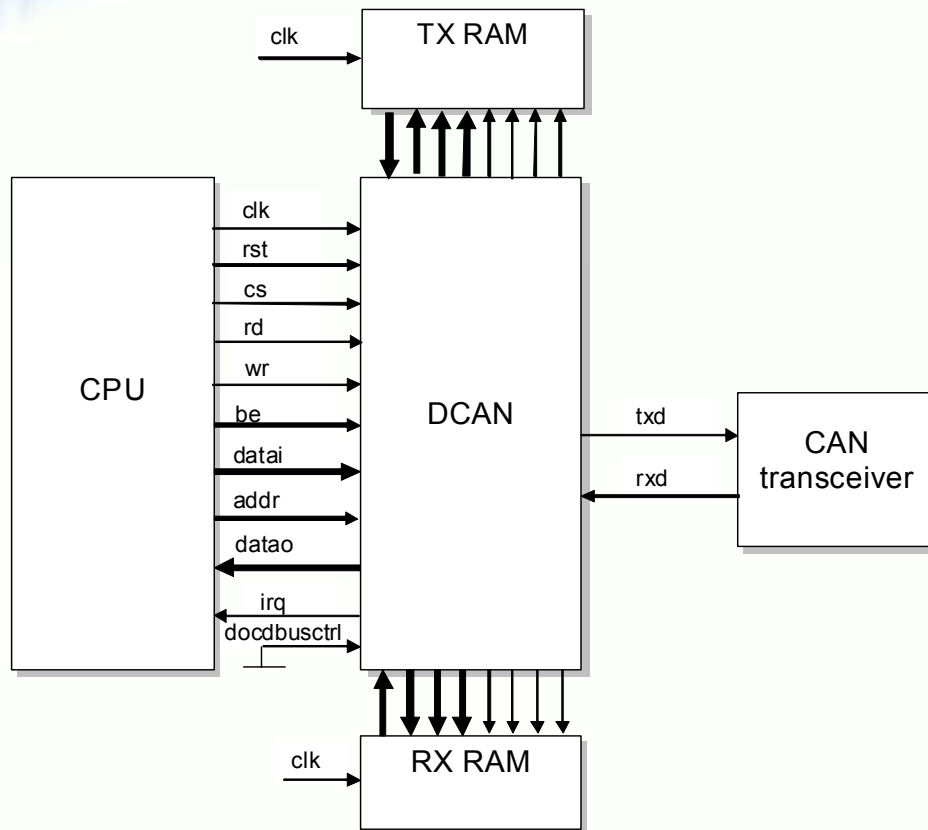
Error Management Logic (EML) – is responsible for fault confinement handling.



Acceptance Filter (ACF) – decides whether incoming messages are accepted or not based upon filter registers settings.

TX/RX RAM interfaces – interfaces to external dual port memories used by the DCAN core to store received and transmitted frames.

DSPI allows direct interface to almost any existing synchronous serial peripheral.



CONTACT

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