

Audio Platform

USB 2.0 Audio Design Platform

ver 1.10

OVERVIEW

The USB 2.0 Audio Design Platform is a complete, integrated solution dedicated to use in USB based Audio Devices like speakers or microphone.

The complete Audio Design Platform includes:

- DUSB2 peripheral controller designed to support 12 Mb/s “Full Speed” (FS) and 480 Mb/s “High Speed” (HS) serial data transmission rates
- DP8051XP ultra high performance, speed optimized, fully customizable 8051 8-bit microcontroller with built in DoCD™ debug IP core
- Audio Devices software stack optimized for DP8051XP 8-bit CPU
- FPGA board with ready to use, preprogrammed example USB stereo speakers application
- HAD2 – DoCD™ Hardware Assisted Debugger board
- DoCD™ Debug Software
- DoCD™ driver for Keil development software
- DoCD™ driver for IAR development software

MAIN FEATURES

- Full compliance with the USB 2.0 specification
- Full-speed 12 Mbps operation
- High-speed 480 Mbps operation
- Supports UTMI Transceiver Macrocell Interface
- Suspend and resume power management functions
- 100% software compatible with industry standard 8051
- Up to 256 bytes of internal (on-chip) Data Memory
- Up to 64K bytes of internal (on-chip) or external (off-chip) Program Memory
- Up to 16M bytes of external (off-chip) Data Memory
- User programmable Program Memory Wait States solution for wide range of memories speed
- User programmable External Data Memory Wait States solution for wide range of memories speed
- Fully synthesizable, static synchronous design with positive edge clocking and no internal tri-states
- Scan test ready

DELIVERABLES

- ◆ DUSB2 & DP8051XP source code:
 - VHDL Source Code or/and
 - VERILOG Source Code or/and
 - Encrypted, or plain text EDIF netlist
- ◆ DUSB2 & DP8051XP test bench environments
 - NCSim automatic simulation macros
 - ModelSim automatic simulation macros
 - Active-HDL automatic simulation macros
 - Tests with reference responses
- ◆ Audio Devices software stack source code
- ◆ FPGA board with ready to use, pre-programmed example application
- ◆ HAD2 - DoCD™ Hardware Assisted Debugger board
- ◆ DoCD™ Debug Software
- ◆ DoCD™ driver for Keil development software
- ◆ DoCD™ driver for IAR development software
- ◆ Technical documentation
 - Installation notes
 - HDL core specification
 - Datasheet
- ◆ Synthesis scripts
- ◆ Technical support
 - IP Core implementation support
 - 3 months maintenance
 - Delivery the IP Core updates, minor and major versions changes
 - Delivery the documentation updates
 - Phone & email support
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LICENSING

Comprehensible and clearly defined licensing methods without royalty per chip fees make using of IP Core easy and simply.

Single Site license option is dedicated for small and middle sized companies making its business in one place.

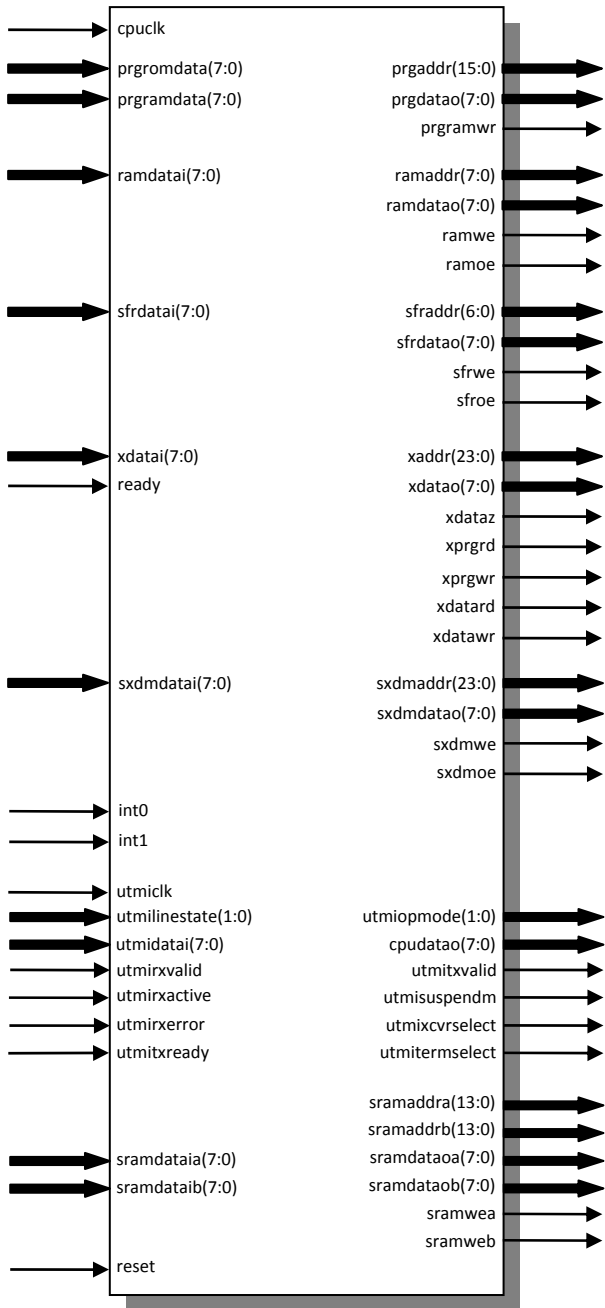
Multi Sites license option is dedicated for corporate customers making its business in several places. Licensed product can be used in selected branches of corporate.

In all cases number of IP Core instantiations within a project, and number of manufactured chips are unlimited. The license is royalty per chip free. There is no time of use restrictions.

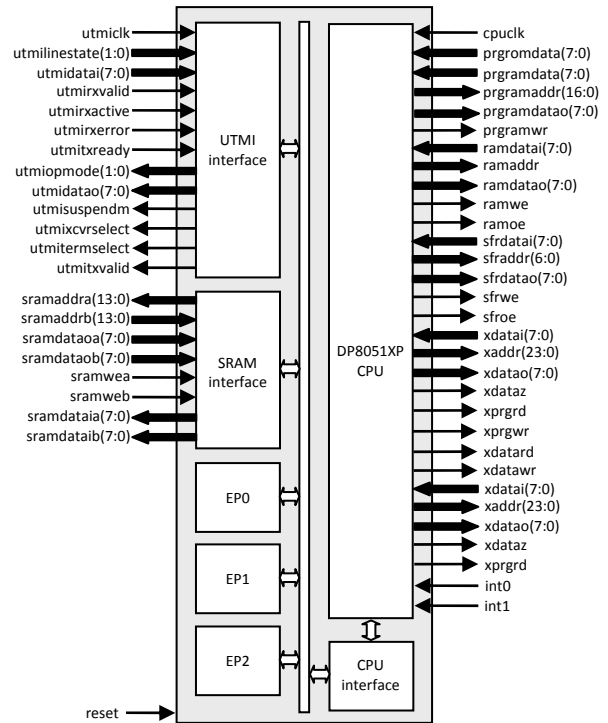
There are two formats of delivered IP Core

- VHDL, Verilog RTL synthesizable source code called HDL Source
- FPGA EDIF/NGO/NGD/QXP/VQM called Netlist

SYMBOL



BLOCK DIAGRAM



PINS DESCRIPTION

| PIN | TYPE | DESCRIPTION |
|--------------------|--------|---|
| reset | input | Global reset |
| utmick | input | USB clock |
| utmilinestate(1:0) | input | USB line state |
| utmidatai(7:0) | input | USB parallel data input bus |
| utmirxvalid | input | USB receive valid |
| utmirxactive | input | USB receive active |
| utmirxerror | input | USB receive error |
| utmitxready | input | USB transmit ready |
| sramdataia(7:0) | input | SRAM port A data input bus |
| sramdataib(7:0) | input | SRAM port B data input bus |
| cpucclk | input | CPU clock |
| prgramdata[7:0] | input | Data bus from internal RAM program memory |
| prgromdata[7:0] | input | Data bus from internal ROM program memory |
| ramdatai[7:0] | input | Data bus from internal data memory |
| sfrdatai[7:0] | input | Data bus from user SFR's |
| xdatai[7:0] | input | Data bus from external memories |
| int0 | input | External interrupt 0 |
| int1 | input | External interrupt 1 |
| utmiopmode(1:0) | output | USB operational mode |

| PIN | TYPE | DESCRIPTION |
|-----------------|--------|--------------------------------------|
| utmdatao(7:0) | output | USB parallel data output bus |
| utmisuspendm | output | USB suspend |
| utmixcvrselect | output | USB transceiver select |
| utmitermselect | output | USB termination select |
| utmitxvalid | output | USB transmit valid |
| sramaddr(13:0) | output | SRAM port A address bus |
| sramaddrb(13:0) | output | SRAM port B address bus |
| sramdataoa(7:0) | output | SRAM port A data output bus |
| sramdataob(7:0) | output | SRAM port B data output bus |
| sramwea | output | SRAM port A write enable |
| sramweb | output | SRAM port B write enable |
| prgaddr[15:0] | output | Internal program memory address bus |
| prgdatao[7:0] | output | Data bus for internal program memory |
| prgramwr | output | Internal program memory write |
| ramaddr[7:0] | output | Internal Data Memory address bus |
| ramdatao[7:0] | output | Data bus for internal data memory |
| ramoe | output | Internal data memory output enable |
| ramwe | output | Internal data memory write enable |
| sfraddr[6:0] | output | Address bus for user SFR's |
| sfrdatao[7:0] | output | Data bus for user SFR's |
| sfroe | output | User SFR's output enable |
| sfrwe | output | User SFR's write enable |
| xaddr[23:0] | output | Address bus for external memories |
| xdatao[7:0] | output | Data bus for external memories |
| xdataz | output | Turn xdata bus into 'Z' state |
| xprgrd | output | External program memory read |
| xprgwr | output | External program memory write |
| xdatard | output | External data memory read |
| xdatawr | output | External data memory write |

UNITS SUMMARY

UTMI Interface – This module is clocked by utmick clock and manages communication with USB 2.0 Transceiver Macrocell. It is responsible for reset detection, speed handshake, token, data and handshake packet reception and transmission.

CPU Interface – This module is clocked by cpuck clock and manages communication with DP8051XP CPU. In this module are located DUSB2 core configuration and status registers.

SRAM Interface – This module manages communication with Synchronous Random Access Memory. It generates address, read and write signals for the SRAM memory and buffers data bytes during the FIFO read and write operations.

EP0 endpoint –The EP0 control endpoint is special bidirectional endpoint used for device configuration and allows generic USB control and status access.

EP1 endpoint – The EP1 data endpoint is unidirectional configurable endpoint used for application specific data transmission.

DP8051XP CPU – Ultra high performance, speed optimized 8-bit embedded controller, 100% software compatible with industry standard 8051.

PERFORMANCE

The following tables give a survey about the Core area and performance in Programmable Logic Devices after Place & Route.

| Device | Speed grade | cpuclk F _{max} | utmickl F _{max} |
|--------|-------------|-------------------------|--------------------------|
| SC | -7 | 100 MHz | >100 MHz |
| ECP2 | -7 | 80 MHz | >100 MHz |
| ECP2M | -7 | 70 MHz | >100 MHz |
| XP2 | -7 | 60 MHz | >100 MHz |

Core performance in LATTICE® devices

Area utilized by complete, integrated USB 2.0 Audio Design Platform in vendor specific technologies is summarized in table below.

| Component | Area | |
|---------------------|-------------|-------------|
| | [LUT4s] | [FFs] |
| CPU interface | 215 | 170 |
| UTMI interface | 250 | 230 |
| SRAM interface | 110 | 95 |
| EPO endpoint | 145 | 140 |
| EP1 endpoint | 155 | 155 |
| DP8051XP CPU | 1060 | 320 |
| DoCD™ debug IP core | 360 | 270 |
| Total area | 2295 | 1640 |

Core components area utilization in ECP2 and ECP2M families

| Component | Area | |
|---------------------|-------------|-------------|
| | [LUT4s] | [FFs] |
| CPU interface | 240 | 170 |
| UTMI interface | 290 | 230 |
| SRAM interface | 120 | 95 |
| EPO endpoint | 160 | 140 |
| EP1 endpoint | 175 | 155 |
| DP8051XP CPU | 1170 | 320 |
| DoCD™ debug IP core | 400 | 270 |
| Total area | 2555 | 1380 |

Core components area utilization in XP2 family

| Component | Area | |
|---------------------|-------------|-------------|
| | [LUT4s] | [FFs] |
| CPU interface | 200 | 170 |
| UTMI interface | 230 | 230 |
| SRAM interface | 100 | 95 |
| EPO endpoint | 130 | 140 |
| EP1 endpoint | 140 | 155 |
| DP8051XP CPU | 990 | 320 |
| DoCD™ debug IP core | 330 | 270 |
| Total area | 2120 | 1380 |

Core components area utilization in SC family

CONTACTS

For any modifications or special requests
contact to DCD.

Headquarters:

Wroclawska 94

41-902 Bytom, POLAND

e-mail: info@dcd.pl

tel. : +48 32 282 82 66

fax : +48 32 282 74 37

Distributors:

Please check <http://www.dcd.pl/apartn.php>